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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KITOV, ZEEV V	
ART UNIT	**PAPER NUMBER**
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,955	BOUCHER, CRAIG J.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on June 14, 2007. Arguments have overcome the rejection under U.S.C 103(a). An office Action follows.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Muller (US 4,632,032). Regarding Claim 1, Muller discloses an electrical initiation element having signal input nodes thereto (3, 4, upper node of resistor 20, ground); protective circuitry connected across the signal input nodes (21 and 14), the protective circuitry comprising a clamping portion (14) responsive to input signals at the input nodes (upper node of resistor 20) to divert from the initiation element at least a portion of such input signals, the clamping portion being responsive to a release signal to permit the input signal to pass to the initiation element upon receipt of such release signal; and a timer portion (10, 9, 20, 19) connected to the clamping portion (through diode 16) and to the input nodes. The timer circuit is being responsive for issuing a release signal to the clamping portion after passage of a clamping interval after the receipt of the input signal, i.e., after reception of the input signal (3) the control circuit (2) issues two control signals, an

upper signal starts blocking the supply of the controlling voltage (through 20 and 16) to the clamping element (14), which being switched off releases the base (12) of the switching element (5). In addition, another output signal from control circuit (4) drives the switching element to a conduction state.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller in view of Pathe et al. (US 6,173,651). Regarding Claims 2 – 4, Muller discloses two time delay circuits (11 and 18). However, it does not disclose the time delay durations. Pathe et al. disclose the time delay in detonator control being set from 1 msec. to 3,000 msec. (col. 12, lines 4 – 10). Duration of a first timing interval (circuit 11) should be selected such to prevent penetration of rush currents and spurious voltage associated with connection of the battery (8) into the circuit. Duration of a second timing interval (circuit 18) should be selected such as to prevent premature activation of the detonator (6) (col. 3, line 61 – col. 4, line 2). Therefore, the time delay durations are a result effective variable, i.e., a variable, which achieves a recognized result and which may be optimized by experimenting. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Muller solution by

setting the time delay to some specific values such as for example, between 20 and 100 microseconds, because as Court Decision *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) states: "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

Regarding Claim 5, Pathe et al. disclose a timer circuit including EEPROM circuit, which as well known in the art, is built with MOS technology. According to The Authoritative Dictionary of IEEE Standard Terms, the unipolar transistor is "a transistor that utilizes charge carriers of only one polarity". Therefore, the MOSFET is a proper unipolar transistor. As to bipolar clamping transistor of Muller (14), replacing this bipolar transistor with the unipolar, i.e., MOSFET-type transistor is a matter of the designer choice. Each type of transistors has its own advantages and disadvantages, and it is up to the designer to choose one of them according to other Specification requirements. The choice is limited to only two types of transistors and the results of the choice are quite predictable. The selection of the unipolar transistor for the time delay element and for the clamping transistor would have been obvious because the substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Claims 6 - 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller in view of Aikou et al. (US 4,712,477). Claim 6 differs from Claim 1 rejected above by its limitation of bipolar clamping circuit and bipolar timer circuit. Muller

discloses the bipolar clamping circuit (14). Aikou et al. disclose the timer circuit (7, 8, 9, 5, 6 and 2 in Fig. 1), which includes the comparator (2 in Fig. 1) built with bipolar transistors (Fig. 3). The reference has the same problem solving area, namely providing the delay element for detonator. It is actually applying a known technique to a known device ready for improvement to yield predictable results. In the instant case, well known RC delay element being improved by adding a differential comparator circuit built with bipolar transistors, rather than using as comparator the emitter-base junction of the switching transistor; such modification improves a precision and a thermal stability of the delay. The claim would have been obvious because using a comparator at the output of the RC delay circuit was recognized as part of the ordinary capabilities of one skilled in the art. As to use of bipolar transistor rather than MOSFET, even though in modern electronics the circuits are mostly built with MOSFET based integrated circuits, in non-integrated components design the bipolar transistors are still sometimes used. Since a choice in selection of particular type of transistor is limited to either field-effect or bipolar transistors, and results of such selection are quite predictable, such selection does not present an innovation.

Regarding Claim 7, Aikou et al. disclose the electronic delay detonator built in form of integrated circuit (Fig. 1). In modern electronics a tendency to integrate the electronic circuit are common among designers. The claim would have been obvious because a particular known technique, i.e., integration of the electronic circuits, was recognized as part of the ordinary capabilities of one skilled in the art. The advantages of integration are well known as well.

As per Claim 8, it differs from Claims 1 and 7 rejected above by its limitation of some structural details of mounting the initiation element and the protective element. Pathe et al. disclose an electro-explosive device having the initiative element and protective circuit being mounted on a header (4 in Fig. 1) with two electrical leads (16a and 16b in Fig. 1) connected to the electronic protective circuit (15 in Fig. 1) and further including a shell (2 and 5 in Fig. 1) mounted an the header and a charge of reactive material (11 in Fig. 1) in the shell. The claimed structure includes well-known elements used according to their specifications and interconnected in a known way so that the results of such arrangement are well anticipated. The claim would have been obvious because a particular known technique of arranging the electronic protective circuit in the shell together with electrical leads and reactive material was recognized as part of the ordinary capabilities of one of ordinary skill in the art.

Regarding Claim 10, Aikou et al. disclose the initiation element is (16 in Fig. 1) responsive to an input signal at the input nodes (10 and 11 in Fig. 1) that exceeds a function time of the initiation element by at least as much as delay time of the time delay element (7, 8, 9, 5, 6 and 2 in Fig. 1), the function time of the initiation element being a time sufficient to cause initiation of the initiation element. Satisfaction of such limitation is inherent in the structure of Aikou et al. reference since otherwise the system would not work. In the Muller system modified according to teachings of Aikou et al. the signal passing the clamping element must have duration exceeding the clamping time. A motivation for modification of the primary reference is the same as above.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller in view of Li et al. (US 5,689,133). Claim 9 differs from Claim 1 rejected above by its limitation of an over-voltage protection. Li et al. disclose the over-voltage protection circuit (Fig. 4A) wherein the clamping portion (T124 in Fig. 4A) is responsive to an input signal at the input node (in PAD 101 in Fig. 4A) to divert from the signal from passing further to the processing circuit a first portion of the input signal above a defined threshold (of zener Z124 in Fig. 4A), while permitting a second non-zero portion of the input signal to pass further to the processing circuit. The reference is pertinent for the case since it discloses the over-voltage protection of the input signal line by clamping the line. In Muller circuit the clamping element is (14). The claim would have been obvious because a particular well-known technique of over-voltage protection by clamping the signal line when the signal voltage exceeds the predetermined value was recognized as part of the ordinary capabilities of one skilled in the art; and an application of this technique brings quite anticipated results.

Response to Arguments

Applicant Arguments have been given careful consideration but they are moot in view of new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach

examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry, can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
08/07/2007

8/19/07

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER